Mixed-Mode Class AB Neuron Building Blocks: Analysis and Real Application

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Abstract—This paper explains the design and simulation of basic blocks to build a mixed-signal current mode artificial neural network: a class AB current follower, a four quadrant multiplier using a transistor-based current divider and a class AB current mode activation function. Also the simulation results of a neural network model, made up of processors using these elements applied to a small sensor linearization problem are presented. System simulation results and application performance applied to four different temperature sensor samples are shown.

***Index Terms*—Mixed-Mode Artificial Neuron, Mixed-Mode Four-Quadrant Multipliers, Current-Mode Activation Function, Analog Sensor Linearization.**

I. INTRODUCTION

ARTIFICIAL Neural Networks (ANNs) are computing tools based on the mammalian nervous system operation. Basically it consists of small processing elements, called artificial neurons, highly interconnected and arranged in layers. The input-output function carried out by these systems is learned by means of a training process where input-output data pairs are iteratively presented, adjusting the system free parameters (called weights) that connect inputs from a neuron layer with the preceding neuron layer outputs. ANNs can be implemented in several ways, depending on the application requirements. Thus, in systems where size, power consumption and speed are main requirements, electronic analog implementation is a suitable selection [1]. Today, shrink bias voltages make difficult to processing high resolution data in voltage-mode. In this case, current-mode processing gives better results at lower bias, reducing the power consumption [2].

On the other hand, analog implementation of reliable long-term and mid-term analog programmable weights results very hard due to mismatching and offsets. Due to the high accuracy of digital storing data for long and mid-term in register-based structures, the combination of both electronic technologies can improve the system features. Previous works [3] have presented the use of mixed-mode multipliers in artificial neuron implementation, showing promising results applied to real problems.

In Section II this paper presents the proposed design of the building blocks of a current mode class AB digital weight neuron; Section III presents simulation results of an architecture of a mixed signal artificial neural network made up with these elements; Section IV shows the results of applying this neuron model to a real problem, the linearization of a negative temperature coefficient resistor (NTC); Finally the conclusions of this work and future work are presented.

II. BUILDING BLOCKS IMPLEMENTATION

The proposed neuron building blocks have been implemented using the Austria Microsystems (AMS) 0.35µm design kit. Maximum processing currents are limited to ±50µA, voltage bias are limited to 3.3V in the inverters and ±2V in the rest of the multiplier structure.

A. Mixed Signal Four-Quadrant Multiplier

The proposed multiplier structure can be seen in Fig. 1. It is composed of a 7-bit digitally programmable current divider, a class AB current follower, whose scheme is shown in Fig. 2 and a multiplexer that controls the current path according to the sign bit of the digital operand. When

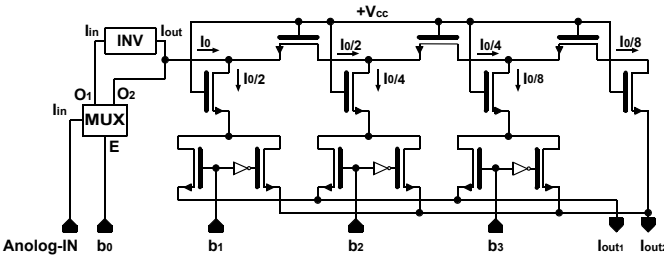

Fig. 1. 3–bit four quadrant mixed analog-digital multiplier (ADM).

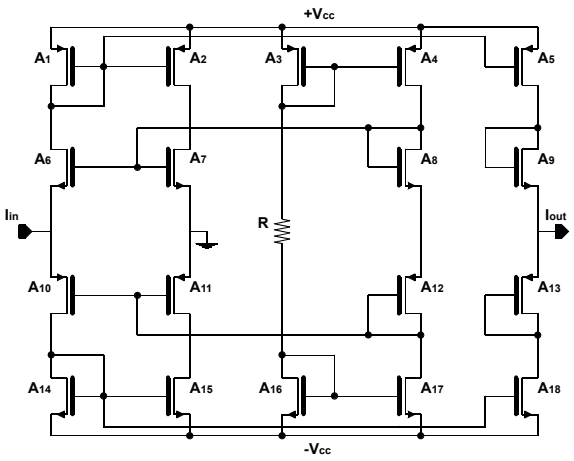

Fig. 2. Class AB current follower.

the weight sign bit is positive (b_0=0V), current goes to the divider straight, but if sign bit is negative (b_0=3.3V), current is driven through the current follower in order to change its direction. Current output ranges from I_{in} to $-I_{in}$.

1) Programmable Current Divider

The main four-quadrant multiplier building block consists of an R-2R ladder structure [4] implemented with NMOS transistors. This structure (Fig. 1), widely presented in the literature [5], [6], [7] allows the current to flow in both directions and is designed using identical 0.3µm length and 10µm width transistors working in triode mode. Gate voltages b_i (Fig. 1) control the current flow through the right-side transistors (b_i=0V) or through the left-side transistor (b_i=3.3V). For N bits, output current is described according to

$$I_{out_1} = I_0\left(\frac{1}{2^N} + \sum_{n=1}^{N}\frac{\bar{b}_n}{2^n}\right) \quad (1)$$

$$I_{out_2} = I_0\left(\sum_{n=1}^{N}\frac{b_n}{2^n}\right) \quad (2)$$

where I_{out1} and I_{out2} are the lower and upper output currents. In our work, I_{out2} has been selected as the final output current. Thus, according to (2), digital weight absolute ideal value ranges from 0 to $1\text{-}1/2^N$. Assuming a seven bits plus sign weight representation, theoretical digital operand minimum module value equals to $7.8125\cdot10^{-3}$.

2) Current Follower

Multiplier sign bit is implemented using a class AB current follower scheme presented in [8] (Fig. 2). This structure gives a zero centred low-distortion current follower using a ± 2V bias voltage. Tables I and II show the current follower design characteristics and transistor sizes, respectively. The bias current value (30µA, see Table I) ensures a very low distortion in the processing signals range [9]. The resistor value in the middle of the structure is 66.66kΩ.

B. Non-Linear Activation Function

Activation function circuit consists of a class AB current conveyor (Fig. 3), similar to the circuit proposed in [10]. Circuit output has *tanh* type behaviour. Design characteristics and transistor dimensions are shown in Tables III and IV respectively.

TABLE I
CURRENT FOLLOWER DESIGN CHARACTERISTIS

$\pm V_{cc}$(V)	±2
Ibias(µA)	30
V_{gs}(V)	±1
V_{ds}(V)	±1

TABLE II
CURRENT FOLLOWER TRANSISTOR DIMENSIONS

Transistor	W(µm)	L(µm)
A_1, A_2, A_3, A_4, A_5	4.25	0.3
A_6, A_7, A_8, A_9	13.00	0.3
A_{10}, A_{11}, A_{12}, A_{13}	48.15	0.3
A_{14}, A_{15}, A_{16}, A_{17}, A_{18}	0.85	0.3

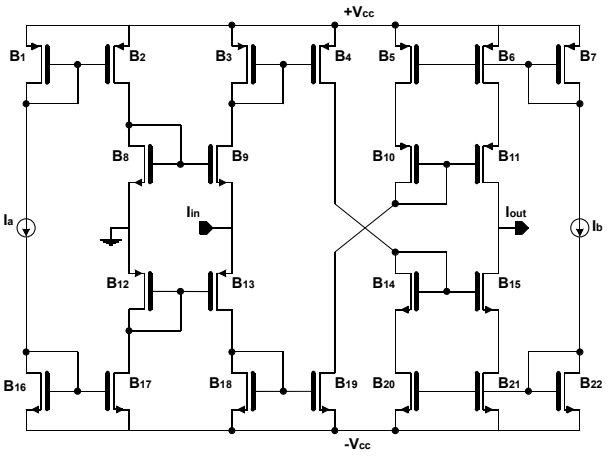

Fig. 3. Class AB activation function.

III. BUILDING BLOCKS SIMULATION

Artificial neuron circuit simulation was carried out using two different simulators (Spectre and Hspice) using Cadence Design Framework, obtaining similar results.

A. Mixed Signal Four-Quadrant Multiplier Results

Table V shows results of the current follower simulation. As can be seen, the circuit shows a 5% loss current (slope is not 1) that can be reduced replacing the simple current mirrors used in the design with cascode current mirrors. On the other hand, offset effects are very low.

The mixed-mode multiplier behaviour has been numerically modelled using Matlab. Practical multiplier operation can be represented by:

$$out = 0.974865wp - 0.0136726p \quad (3)$$

where w is the digital weight and p is the analog current

TABLE III
ACTIVATION FUNCTION DESIGN CHARACTERISTICS

$\pm V_{cc}$(V)	±2
I_a(µA)	5
I_b(µA)	50
V_{gs}(V)	±1
V_{ds}(V)	±1

TABLE IV
ACTIVATION FUNCTION TRANSISTORS DIMENSIONS

Transistor	W(µm)	L(µm)
B_1, B_2, B_3	0.9	0.3
B_4	5.35	0.3
B_5, B_6, B_7	6.9	0.3
B_8, B_9	1.9	0.3
B_{10}	2.85	0.3
B_{11}	0.65	0.3
B_{12}, B_{13}	8.7	0.3
B_{14}	0.7	0.3
B_{15}	0.6	2.1
B_{16}, B_{17}, B_{18}	0.6	1.7
B_{19}	1.2	0.3
B_{20}, B_{21}, B_{22}	1.4	0.3

TABLE V
CURRENT FOLLOWER SIMULATION RESULTS

I_{off}(nA)	0.74
V_{off}(µV)	65
Slope	0.951166

input to the analog-digital multiplier. Results are shown in Fig. 4. Fig. 5 presents the differences between the ideal operation and the realistic operation of the multiplier.

B. Non-Linear Activation Function Results

Non-linear output function is modelled using a 1-15-1 Multilayer Perceptron (MLP). Simulation and ideal *tanh* output functions are shown in Fig. 6. Differences between simulated circuit and ideal output are presented in Figure 7.

IV. REAL APPLICATION EXAMPLE: SENSOR LINEARIZATION

The following example has been widely analyzed in the literature [11], [12], [13]. It consists in conditioning the response of a nonlinear sensor with sigmoid output using a MLP. There are diverse sensors with this output characteristic form (such as giant magnetoresistive sensors [14]). In this work, we have used the well-characterized negative temperature coefficient resistor (NTC) connected on a resistive divider, which voltage output is shown in Fig. 8. In this case, the MLP output provides the correction that must be added to the sensor characteristic to linearize the total behaviour.

In order to verify that results are independent of the sample we used four datasets from four different NTC sensors, training the network for each one of them.

Patterns of each NTC consist of 71 sensor output voltages collected in the 253-323K temperature range.

For each NTC, data are divided in two datasets, consisting of 61 patterns for the learning process and 10 patterns for the verification phase. These validation patterns are randomly selected from the whole dataset.

A. Network Architecture

Previous works [3] show that a 1-1-3-1 MLP network architecture gives the best performance results in this case. The used neural network scheme is shown in Figure 9. Output function of the first hidden and output layer neurons are linear, while the neurons in the second hidden layer have the designed *tanh* circuit as output function. All of them use the analog-digital multiplier presented in Section II. The use of the realistic multiplier model and non-ideal activation function makes necessary to double the number of hidden neurons, compared to the use of ideal elements in the neuron definition. On the other hand, accuracy in digital weights must be carefully selected. Considering circuit size restrictions and minimum accuracy, an 8-bit representation of the weights (with positive and negative codification) gives a good system performance.

B. Training Results

The resulting artificial neural network is trained on a computer. Our experience confirms that learning algorithms based on error back-propagation have demonstrated a worse efficacy in network weight adaptation in systems with high non-linearities and offsets, compared to perturbative techniques [15], [16] These methods estimate output error variations due to small random weight changes. If a random variation makes the error to decrease, the weight change is accepted; otherwise, weight remains unchanged. This methodology is not dependent on the arithmetic operations

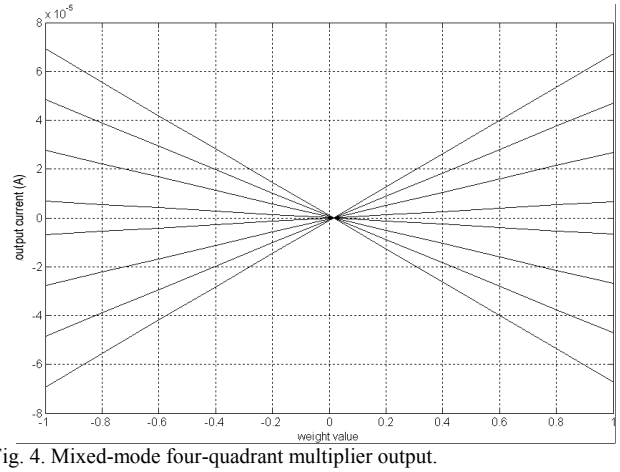

Fig. 4. Mixed-mode four-quadrant multiplier output.

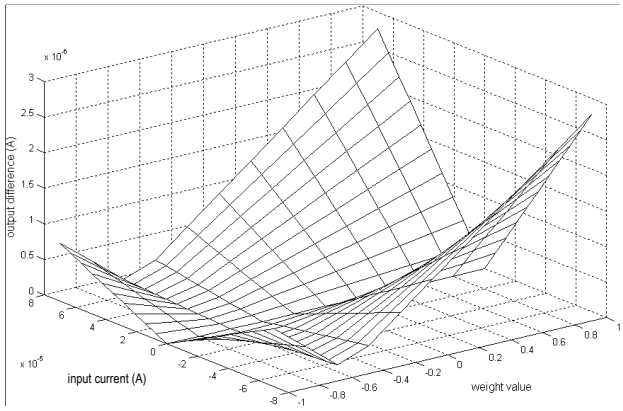

Fig. 5 Differences between the ideal and simulated mixed-mode multiplier.

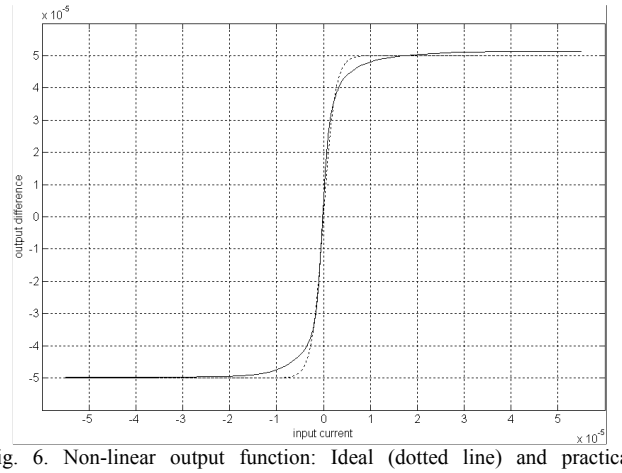

Fig. 6. Non-linear output function: Ideal (dotted line) and practical (continuous line).

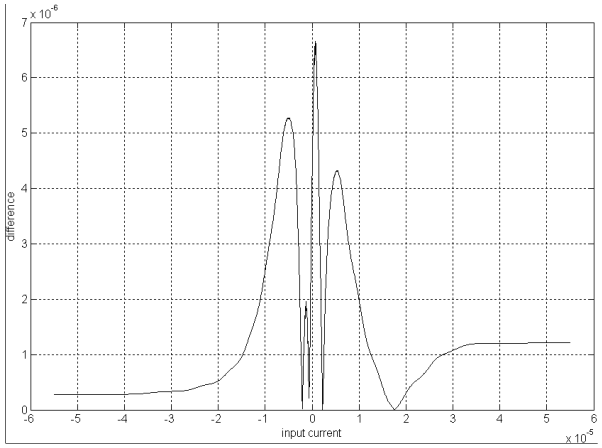

Fig. 7. Differences between the practical and ideal operation of the activation function.

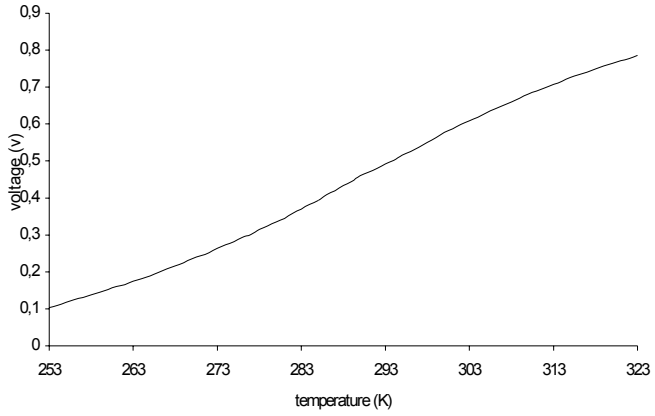

Fig. 8. NTC output voltage (connected on a resistive divider).

carried out by the artificial neuron. However, in standard back-propagation algorithms the use of different arithmetic operations can change drastically the network learning behaviour.

Although there are proposed in the literature several parallel perturbative algorithms developed for systems with digital weight storage [17], the learning algorithm applied in this work is based on the classical serial weight-perturbation algorithm presented in [18].

Fig. 10 shows the corrected output voltage compared to the ideal expected output (dashed line) after 8-bit resolution weight discretization. As this figure shows, the output error remains lesser than 1K between 250K and 310K.

The ANN generalization ability is analyzed using the validation dataset and the corresponding network output. In all four examples, output error keeps lower than 1K in the same range from 250K to 310K (Figure 11).

V. Conclusions and Future Work

In this paper the mixed signal class AB neuron basic building blocks are presented. These elements are: a four-quadrant analog-digital multiplier (made of a 7-bit transistor-based current ladder and a class AB current follower) and an activation function. All these elements have been designed using the 0.35µm AMS design kit. In order to validate the use of these circuits in real-world applications, a neural network model was developed using the simulation results of these basic elements. A classic linearization problem was tackle: four different temperature sensors linearization. Results show an application range extension (error lower than 1 degree) of 50% or more.

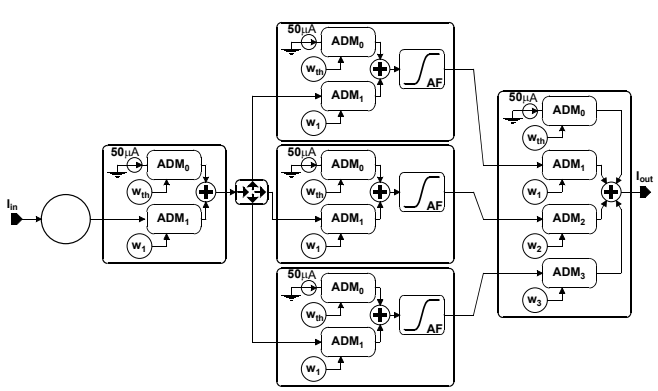

Fig. 9. MLP architecture.

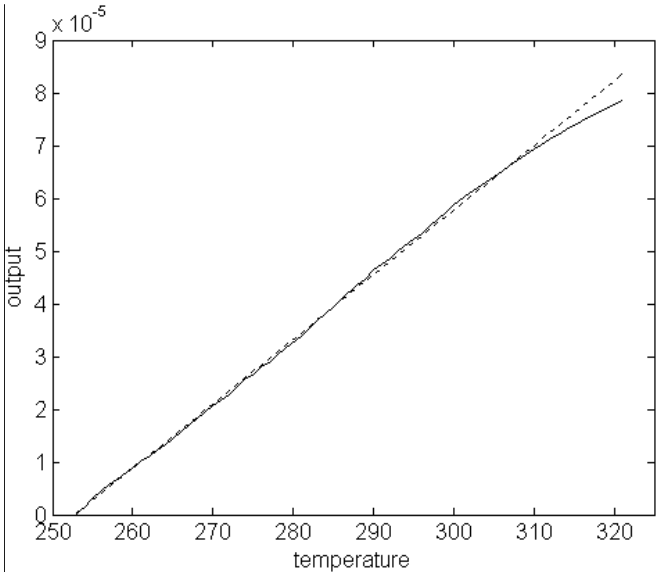

Fig. 10. Corrected output voltage versus ideal linear output.

The next goal is to reduce the output error drift at the end of the sensor span (from 310K to 325K), modifying the design and minimizing the effects of mismatching and offsets.

Acknowledgment

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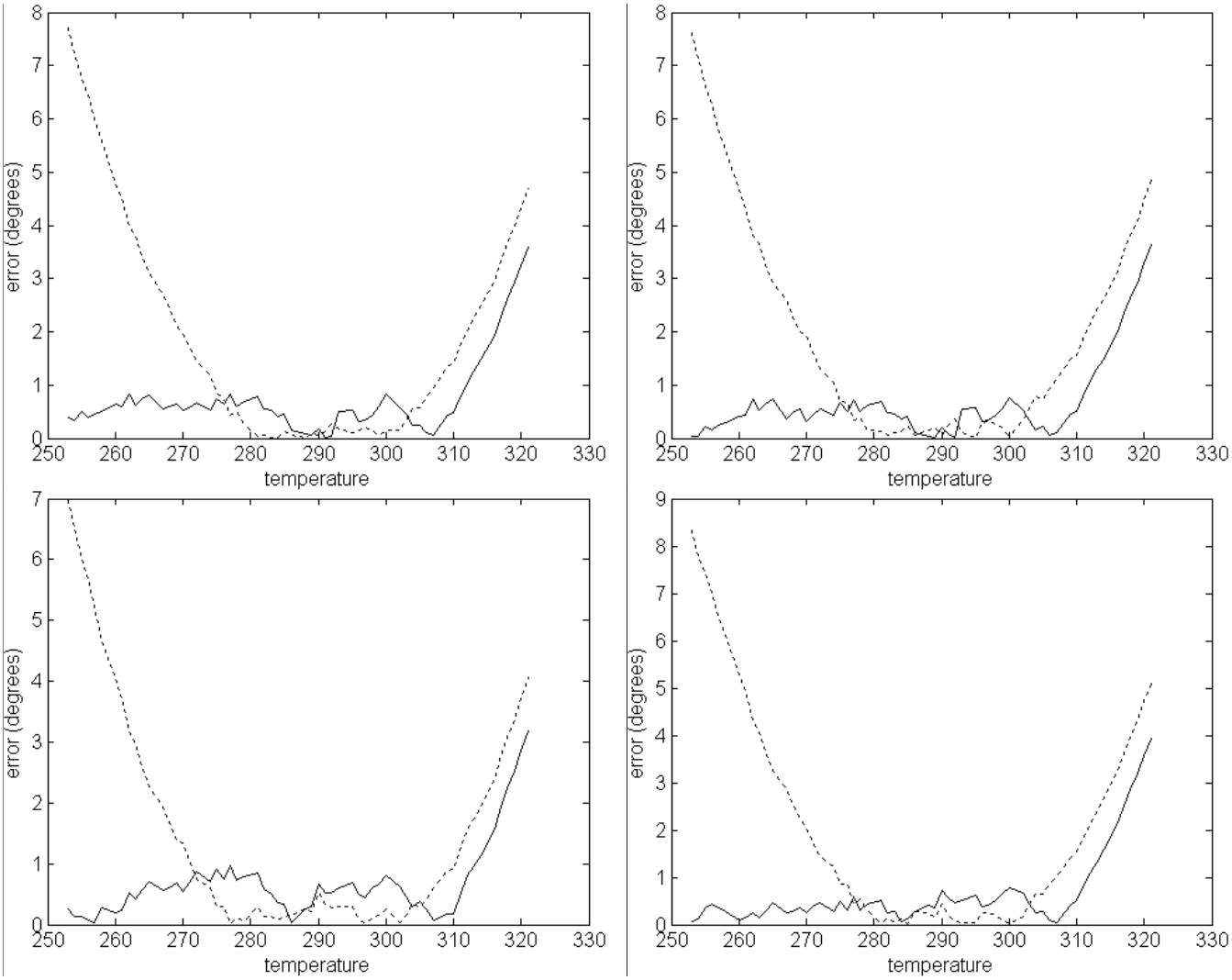

Fig. 11. NTC output error compared to neural network output error for four different NTC sensors.

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